Chapter 7

Design-for-Test

Arnaud Virazel

virazel@lirmm.fr

Why?

- To ensure that a circuit (or system) is testable (technical and financial aspects)
- Test cost
  - Automatic Test Pattern Generation
  - Fault simulation
  - Tester (ATE), test equipment (investment)
  - Test time (effective time on the tester)

Objectives

- **Reduce** the time to market
  - by making the test vector production phase easier (or even automated)
- **Reduce** the test cost
  - by generating smaller test sets
- **Improve** the quality of the test
  - by increasing the fault coverage

DfT Techniques

- Ad-hoc techniques
  - common sense rules from experience
- Structured techniques
  - facilitate access to internal memorization points
  - standard for testing boards and systems
  - can be automated

Ad-hoc Techniques

- Initialization of memory points
- Logic partitioning
- Clock isolation
- Test point insertion
- Facilitate access to buses
- Make the circuits easily initializable
- Polarize the tri-state buses
- Avoid asynchronous circuits

Logic Partitioning

- CPU time for test pattern generation about G^n order (G number of gates and $2 < n < 3$)
- Divide and conquer approach
  - p partitions of G / p gates
  - Ex: original circuit with G = 10000

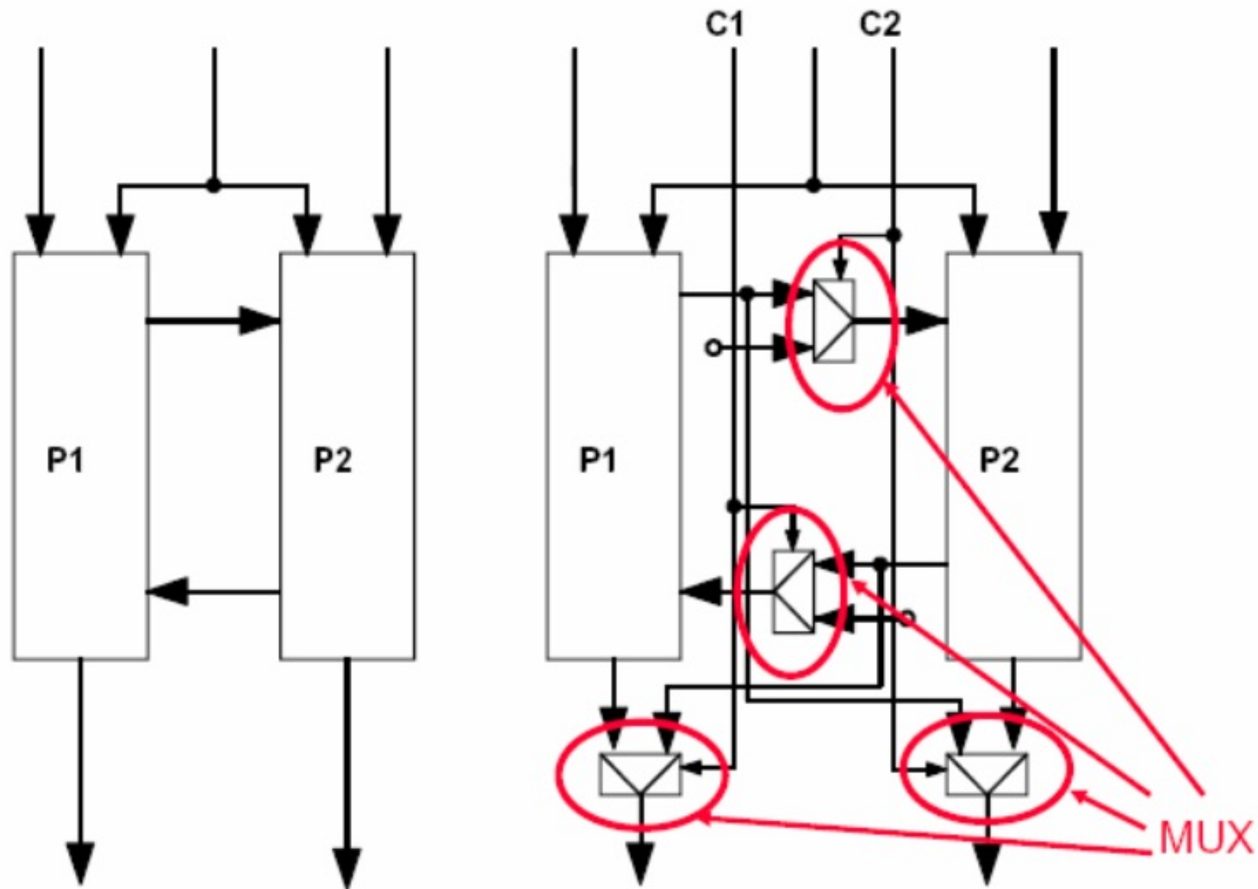
    $\Rightarrow$ CPU time: $G^2 = 10^8$

    2 partitions G_1 and G_2 of 5000 gates

    $\Rightarrow$ CPU time: $G_1^2 + G_2^2 = 5.10^7$

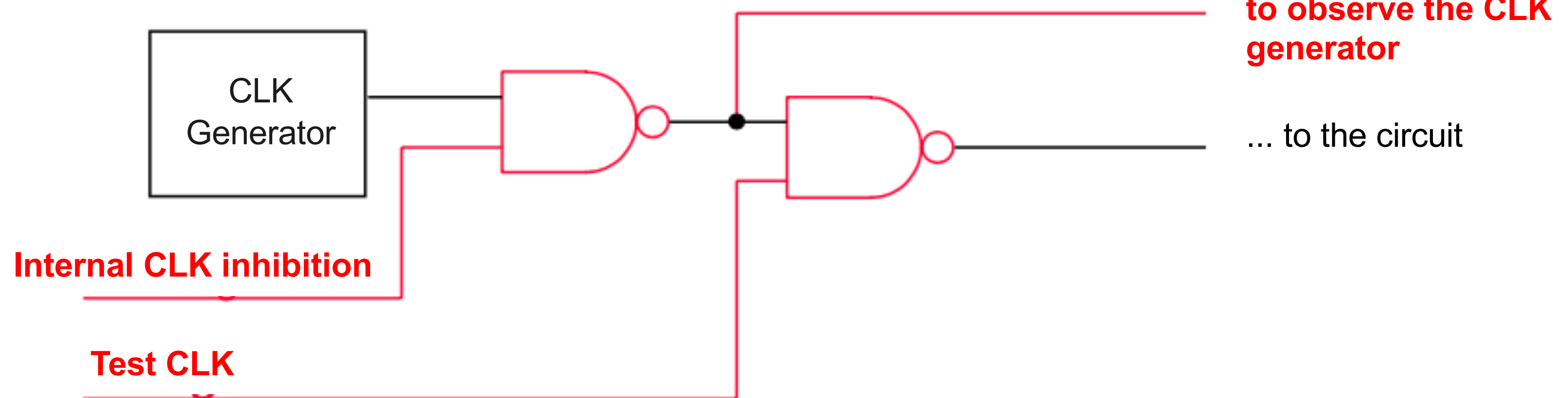
    $\Rightarrow$ 2 times shorter
  - gain of p^{n-1} times ($p \times (G/p)^n$ compared to G^n)
  - partition into logically independent parts

Logic Circuit Partitioning

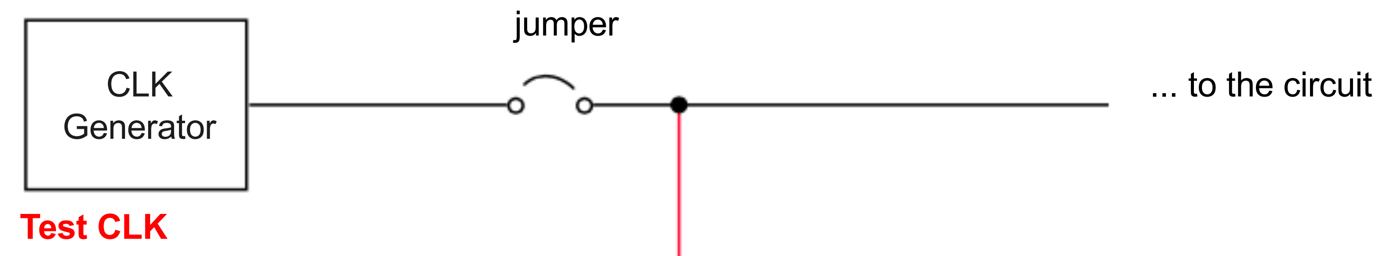


Clock Isolation

- Logic isolation

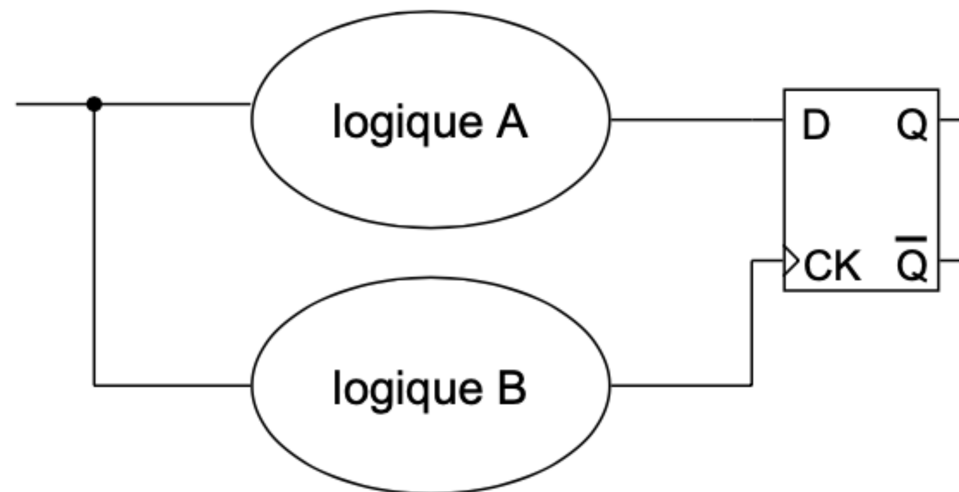


- Hardware isolation



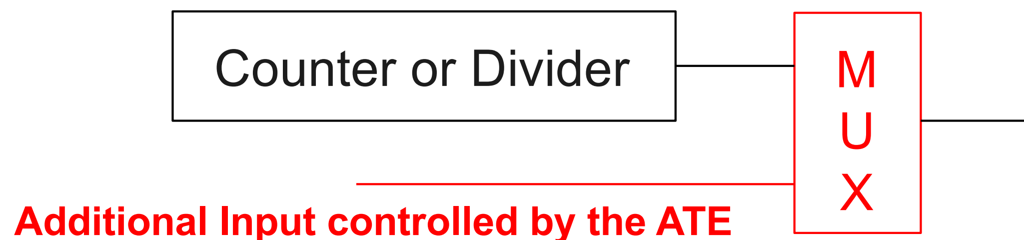
Critical Problem

- CLK and data generated by the same signal
- Sequencing is function of logics A and B delays (variability issue)
- Unpredictable results



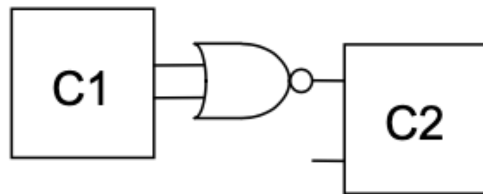
Counter Bypass

- Counters and frequency dividers increase sequential complexity
- Ineffective for ATPGs and testers
- Solution: multiplex the output with a signal that is easier to control by the ATE

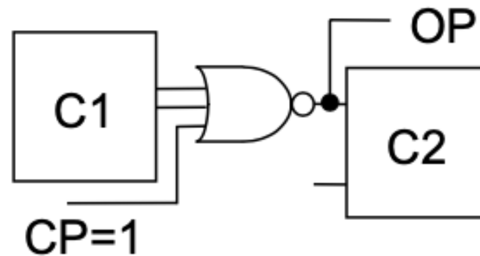


Test Point Insertion

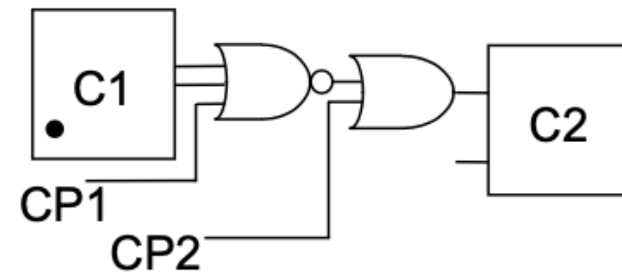
- Improved controllability and observability
  - reduction in the number of vectors
  - improved diagnosis
- Increase in the number of I / O
  - additional pads



Original Circuit



Control at 0
and Observability



Control at 0 and 1

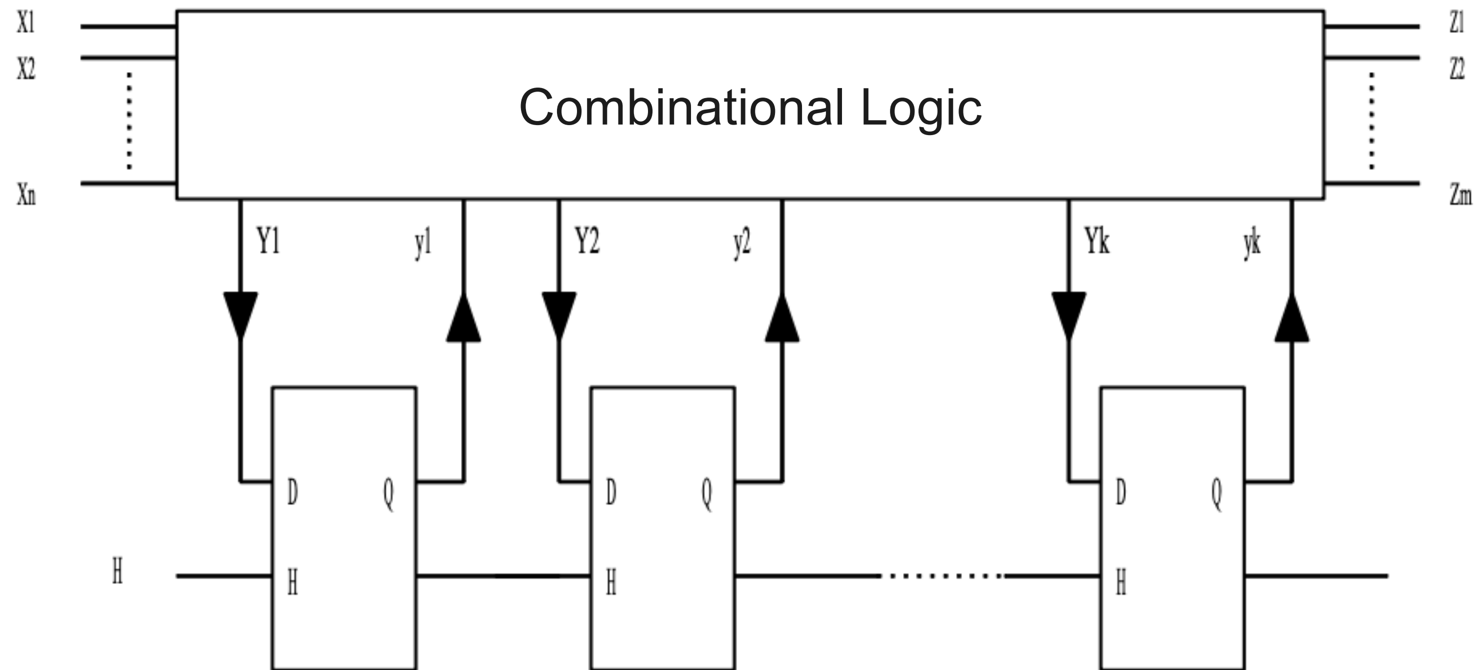
Where to Inject?

- Controllability
  - inputs of sub-circuits that are difficult to control
  - initialization inputs of storage element
  - control of three states
  - Control of multiplexers
  - enable and R / W of memories
  - return loops
- Observability
  - outputs of sub-circuits that are difficult to observe
  - inaccessible control lines
  - serial output of shift registers
  - clock lines
  - return loops

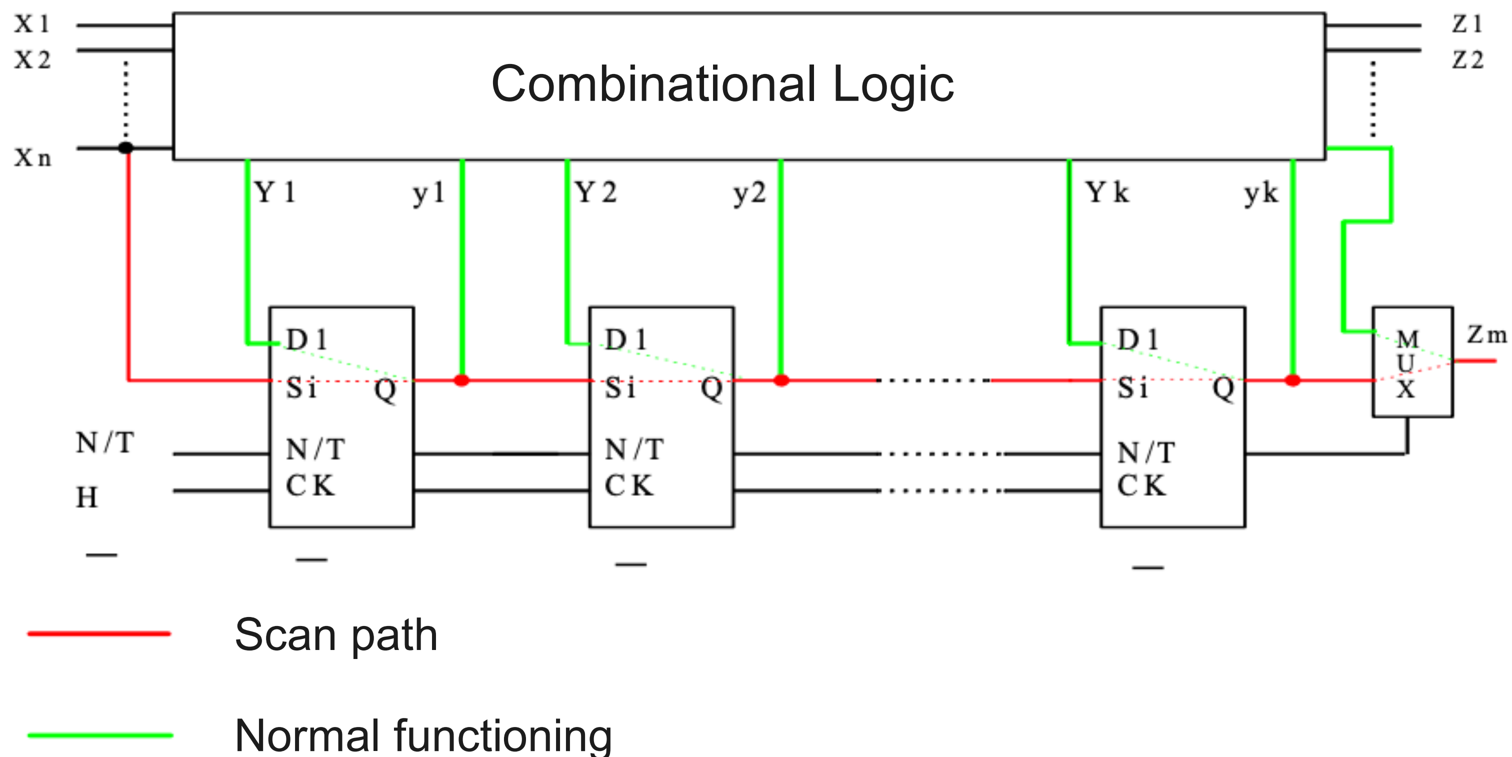
Scan Path

- Objectives
  - Make all flip-flops fully controllable and observable
  - Make the sequential circuit testing ”equivalent” to combinational one

Sequential Circuit



Scan Path Insertion



- Flip-flop modification (additional mux)
- Creation of a shift register (scan chain) allowing full observability and controllability of all storage nodes

Scan Test Procedure

0) Test of the scan chain (sequence of k times 01)

1) Place the circuit in test mode (N / T = 1)

2) Shift-in the test vector {y1, ..., yk} inside the scan path

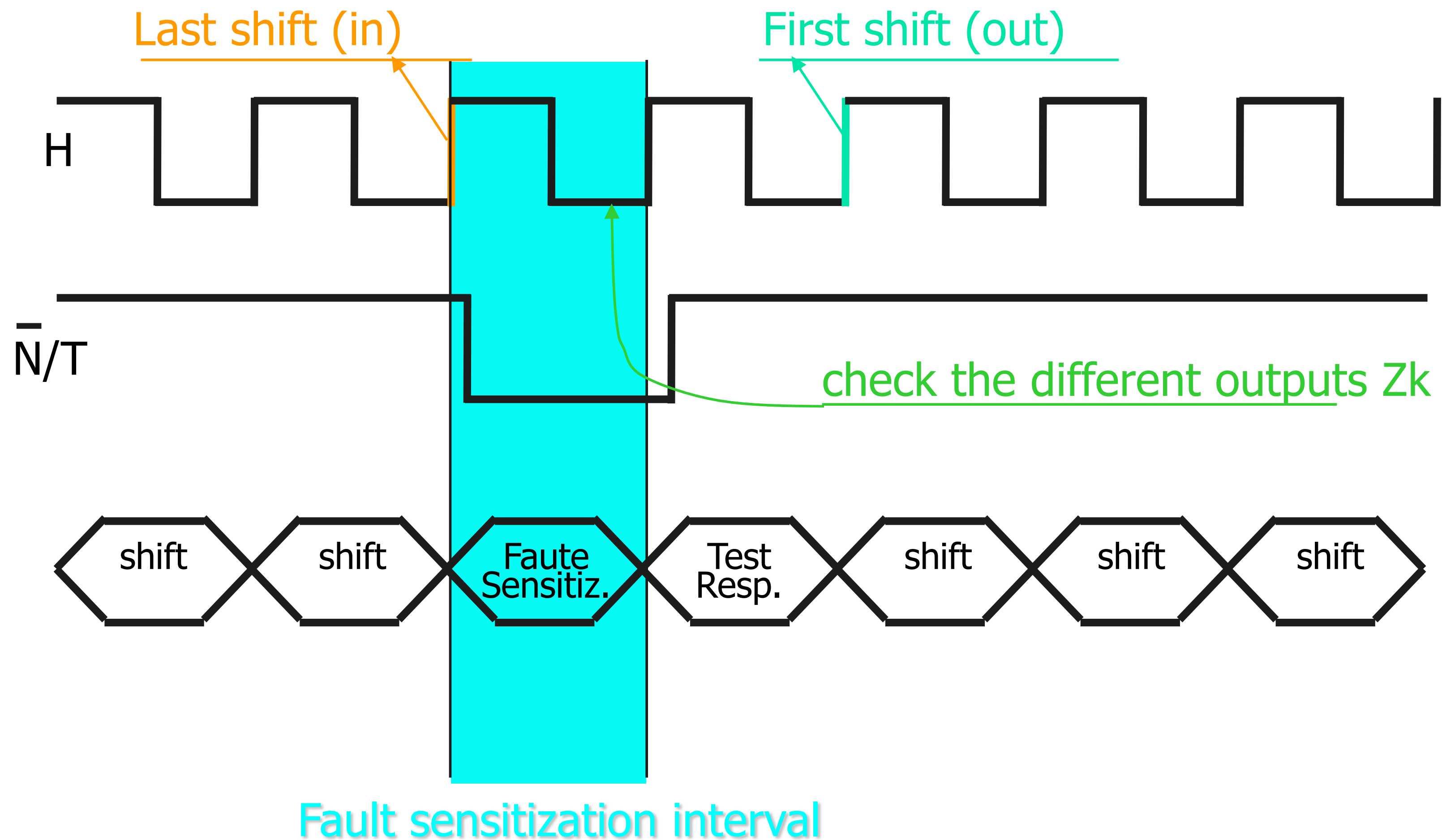
3) Set the corresponding test values on the primary inputs Xi

4) Place the circuit in functional mode (N / T = 0) and after a time necessary for the stabilization of the outputs of the combinatorial part, check the different outputs Zk

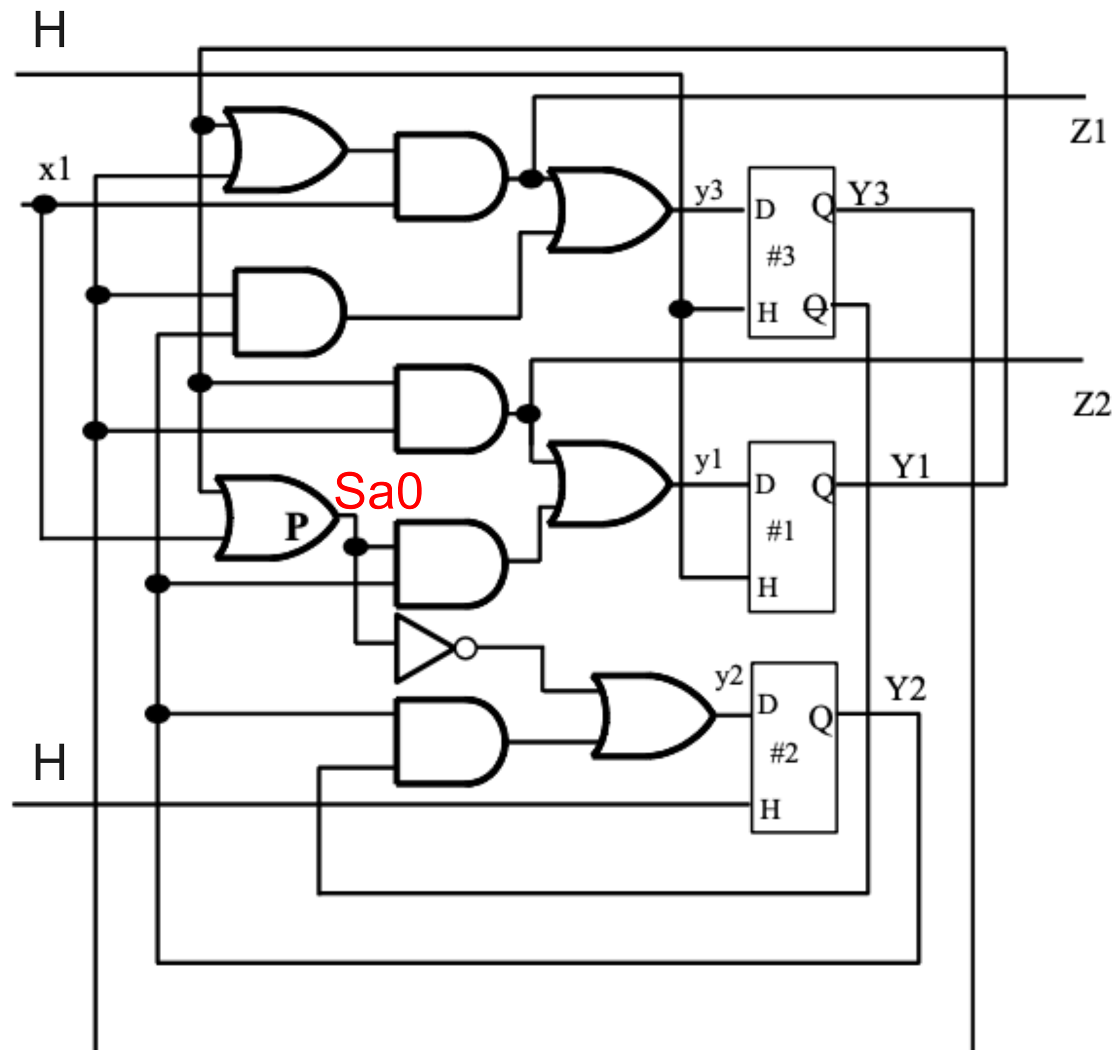
5) Apply a clock pulse to capture the test responses into the scan chain

6) Place the circuit in test mode (N / T = 1) and the contents of the shift register via the output Zm and compare it with the expected results (shift-in at the same time the next test vector)

Waveform

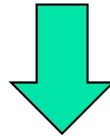


Example



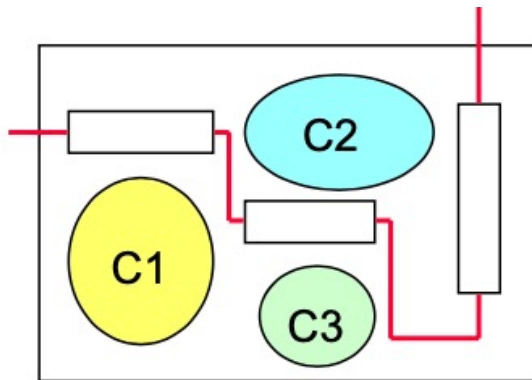
Drawbacks and Solutions

- Area overhead ("Scan" flip-flops, routing, pins)
- Degradation of the nominal operating speed (multiplexers)
- Test time duration of test time: (nb-test) x (nb-FF)

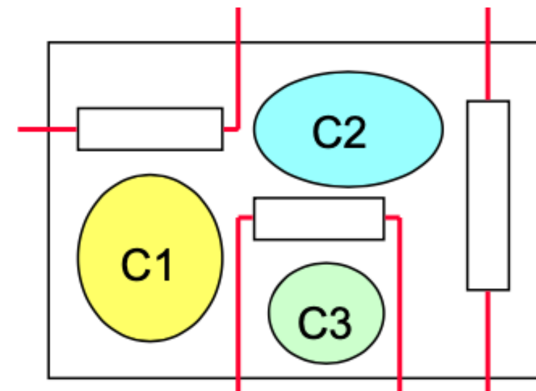


- Different Scan techniques
  - Multiple scan -> STUMP
  - Partial scan

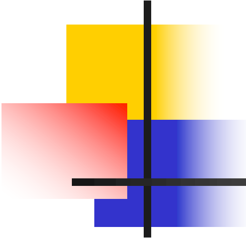
Multiple Scan



- Single Scan chain
  - Reduce number of additional I/O
  - Long test time
  - ATE with a large memory depth



- Multiple Scan chain
  - Reduced test time
  - Reduced ATE memory depth
  - Improved diagnosis
  - Increase in the number of necessary I/O



STUMP Architecture

Edt_top_dnovax_blockname

Input channels

Decompressor

dnovax

Edt_si0

Edt_si1

Edt_si2

Edt_si(n-2)

Edt_si(n-1)

Edt_si(n)

FF FF FF FF FF

Edt_so0

Edt_so1

Edt_so2

Edt_so(n-2)

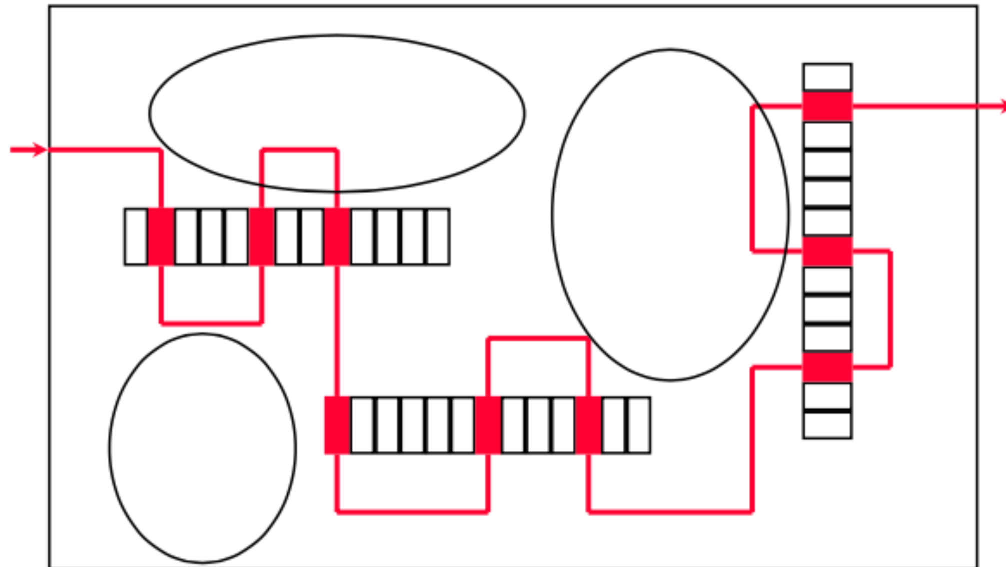
Edt_so(n-1)

Edt_so(n)

Compactor

Output channels

Partial Scan



- All memory elements are not included in the chain
- Require an ATPG for sequential circuit
- Problem of the "good choice" of flip-flops to include in the scan chain
- Less area footprint compared to full Scan
- Time performance improvement

Flip-Flop Selection

- Different approaches based on
  - the use of testability measures (less controllable/observable FFs are selected)
  - the generation of test vectors (propagation and justification phases)
  - the structural analysis (reduction of the depth of sequentiality and number of cycles)
  - a mixed use of these different techniques
- Consideration of constraints
  - critical path for example